REMARKS

This Amendment is in response to the final Office Action dated February 23, 2006. No additional search is required and it is submitted that the case is now in condition for allowance. Clarifying amendments are made to the specification: In paragraph [0039], the sentence "The stack structure including the spacer 12 and the isolation layer 10 refers to the spacer trapping structure, as shown in figure 1" is inserted into the last of [0039]. No new matter is introduced.

A. Claims 1, 5, 13, and 14 are not anticipated by Chang:

The Examiner argues that the Chang patent (US Patent No. 5,969,383) discloses (Fig. 1) an NVM cell 10, comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (control gate structure) 16, silicon dioxide layer (first isolation layer) 23, silicon dioxide layer (first spacers) 28, source/drain (source and drain region) 36, 22, and silicide structures (salicide) 42, 44, 46.

The Applicant disagrees with the Examiner. In fact, the present invention is a two-bit cell. Thus, one control gate controls two charge trapping spacers 12. However, Chang is a one-bit cell including a control gate 35 formed on ONO layers (23, 24, 28). Chang uses one select gate 16 to select two cells rather than a two-bit cell.

The split-gate FET structure of Chang is structurally different from the nonvolatile memory of the present invention. Chang disclosed a split-gate memory device including a selective gate 16, and two control gates 32 and 35, as well known in the art. The select gate is used to select the cell to be operated by its control gate. However, the control gate is used to control the write, read and erase mode for the device. The select gate cannot be the control gate at all. See Chang at col. 1, lines 38-48. Therefore the select gate 16 is used for selecting operation with the control gate 32 or control gate 35, which is completely different from the control gate in claim 1 of the present invention. Actually, the "control gate" mentioned by the Examiner is not a true control gate, it is a "select gate". In other

words, the select gate is used to select one of the control gate 32 and control gate 35 for operation. Therefore, the control gate in claim 1 is not a select gate.

Although Chang discloses (Fig. 1) an NVM cell containing two ONO stacks 25, each of these ONO stacks 25 is formed by a silicon dioxide layer 23, silicon nitride layer 24, and silicon dioxide layer 28. The ONO stack 25 is formed under the control gates 32 and 35, wherein the control gate 32 and 35 refer to the spacers. As known in the art, the control gate is electrically conducting to control the write, read and erase mode for the device. Therefore, Chang uses the conducting spacers to control the operation mode.

Moreover, the spacer trapping structure in the amended Claim 1 of the present invention is non-conducting and formed on the sidewall of said control gate structure. This spacer trapping structure is used to trap carriers and controlled by the control gate where the spacer is attached. As known in the art, the conducting spacers as control gates cannot provide and will not have the capability to trap carriers as dielectrics. Therefore the spacers as control gates of Chang's 32, 35 are unlike the spacer trapping structure in the amended Claim 1 of the present invention.

Furthermore, the present invention uses the control gate 6 formed on the substrate to control the operational modes rather than the select gate and control gates, i.e. spacers in Chang. Although the location of the spacer trapping structure is located at the control gate of the citation, the control gate cannot perform the function to trap any charges. Thus, Chang fails to teach the feature of the claims.

The Examiner argues that Chang discloses a silicon nitride layer (second isolation layer) 24, which is only a part of the ONO stacks 28 and is different with the second isolation layer of Claim 5. According to the discussion of above, the dependent Claims 5, 13 and 14 are believed to overcome the rejections

B. Claim 2, 3, 6, 7, and 15 to 24 are patentable over Chang in view of Zheng

The Examiner notes that Chang does not disclose a pocket implantation region, however arguing that Zheng discloses (Fig. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. Therefore, the Examiner believes that it is obvious to one of ordinary skill in the art at time of the invention to have a lightly doped drain region in order to relax the electric field and reduce leakage current.

As set forth above, the Applicant disagrees with the Examiner although Zheng disclose the step of doping. Zheng discloses a method of forming a high performance and low cost CMOS device which is completely different from the charge-trapping nonvolatile memory of the present invention and the split gate memory device of Chang. Besides, Zheng fails to teach that pocket ion implantation region can be applied to nonvolatile memory, and Chang fails to teach that the split-gate memory device includes a pocket ion implantation region adjacent to the source and drain region. As discussed in above, Chang fails to teach the claimed invention and the independent claims of the claimed invention can not be expected by Chang. No motivation can be found in the prior art to combine Chang and Zheng to achieve claim 2. The dependency claims overcome the rejections as well.

Regarding claim 3, the Examiner believes that Zheng discloses a first region 30 comprising an N type LDD region 8. The Examiner mentioned that the claim 3 is unpatentable under 35 U.S.C. 103(a).

Since Zheng fails to teach that the lightly doped drain region can be applied to charge-trapping nonvolatile memory, and Chang fails to teach that the split-gate memory device includes a lightly doped drain region adjacent to the source and drain region. As mentioned in above A section, Chang fails to teach the claim 1. Therefore, there is no motivation to combine Chang and Zheng to obtain claim 3.

Regarding claim 6, and 7, the Examiner believes that Chang discloses a silicon nitride layer (second isolation layer) 24. As the argument set forth, since Chang discloses a split-gate FET structure which is structurally different from the charge-trapping nonvolatile memory of the present invention, the obviousness of claims 6 and 7 are therefore overcome.

After carefully reviewing the citations, none of them disclosed the energy gap relation limitation as set in the claims 5-8. The claims can not be expected by the citations. Thus, the dependency claims overcome the rejections.

Regarding claims 15, 18 and 21, the Examiner believes that Chang does not disclose the silicide material including TiSi2, CoSi2, or NiSi. And Zheng discloses silicide layer 16 comprising titanium silicide, cobalt silicide and nickel silicide.

Although Zheng disclose the material of silicide layer 16 used for forming a CMOS device, however, as argument set forth, the independent claim can not be expected by the Chang, thus, the dependency claims overcome the rejections as well.

Regarding claims 17, and 20, the Examiner believes that Chang discloses an NVM cell 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer 14, gate 16, silicon dioxide layer 23, nitride spacer 34,35, source/drain 36, 22, silicide structures 42, 44, 46.

After carefully reviewing the citations, none of them disclosed the energy gap relation limitation as set in the claims 13-14, 16-17, 19-20 and 22-23. The claims can not be expected by the citations. Thus, the dependency claims overcome the rejections.

Since the non-obvious of claim 1 is overcome, thus the non-obvious of dependent claims 2, 17 and 20 is therefore overcome.

C. Claim 4, 8, and 22 thru 24 are patentable over Chang in view of Kasuya and further in view of Zheng:

The Examiner notes that Chang does not disclose a double doped drain region. However, the Examiner argues that Kasuya discloses a semiconductor device comprising a high concentration impurity diffusion region 44, and a low concentration impurity diffusion region 42.

Applicant disagrees with the Examiner. First, as discussed, Chang fails to teach the claimed invention. Kasuya discloses a semiconductor device which is structurally different with the charge-trapping nonvolatile memory of the present invention. Further, there is no suggestion in Kasuya that the semiconductor device can include a pocket implantation region, and there is no description in Chang that the CMOS device can include a double doped drain region. Therefore, there is no motivation to combine Kasuya and Zheng.

Regarding claim 8, both of them fail to disclose the energy gap relation limitation as set in the claims.

Regarding to claim 23, the Examiner believes that Chang discloses an NVM cell 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer 14, gate 16, silicon dioxide layer 23, nitride spacers, 34, 35, source/drain 36, 22, and silicide structures 42, 44, 46.

As the discussion above, Chang does not disclose a double doped region. Besides, there is no description that there can be double doped drain region in the split-gate device of Chang. There is no motivation to combine Chang and Kasuya to obtain claim 23.

Regarding claim 24, since the non-obvious of dependent claim 4 is overcome, the non-obvious of claim 24 is therefore overcome.

D. Conclusion

In view of the forgoing, claims 1-8, and 13-24 pending in the application comply with the requirements of patentability define over the applied art. A notice of allowance is, therefore, respectively requested.

Applicant believes no fees are due with this response. However, if any fee is due for consideration of this response, please charge our Deposit Account No. 50-0665, under Order No. 386998041US from which the undersigned is authorized to draw.

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Respectfully submitted,

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